

Applicant(s): Joseph W. Triepels et al.
Serial No.: 09/519,551
For: DISPLAY DEVICE
Filed: March 6, 2000
Examiner: A. Abdulsalam
Group Art Unit: 2674

PHN 17,326

REMARKS/ARGUMENTS

Claims 1 through 10 are pending in the present application.
Claims 1 to 10 have been amended.

The Action rejected claims 1 to 10 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,838,400 to Ueda et al. (hereinafter "the Ueda reference) in view of U.S. Patent No. 6,172,794 to Burdis (hereinafter "the Burdis reference").

It is respectfully submitted that present claim 1 is patentable over each of the cited references and/or the cited combination thereof.

The Action suggests (1) that the Ueda reference teaches "a substrate which is made of multi-layered flexible pad pattern via holes for electric connection." (See page 2 of Action). It is respectfully noted that the Ueda reference actually teaches "a liquid crystal display device, wherein a first substrate is made of the multi-layered flexible substrate including a pad pattern portion for packaging parts, via holes for electric connections", (emphasis added) (col. 5, lines 9-12). It is respectfully submitted that "a pad pattern portion for packaging parts, via holes for electric connections" does not read on "a laminar substrate with opposed sides, which opposed sides are both provided with electrically conducting patterns that are electrically through-connected via at least one opening in the laminar substrate, wherein said at least one opening is proximate said pixels."

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The Action further suggests (2) that the Ueda reference discloses "a type of substrate, which also consists a surface conductor layer, and has electrical connection through holes." (See page 2 of Action). It is noted that the Ueda reference actually teaches "a second substrate is made of the multi-layered wiring substrate for a display data controller and a power supply unit including electric connecting via holes". (col. 5, lines 14-16). It is respectfully submitted that the foregoing does not read on "a laminar substrate with opposed sides, which opposed sides are both provided with electrically conducting patterns that are electrically through-connected via at least one opening in the laminar substrate, wherein said at least one opening is proximate said pixels."

The Action still further suggests (3) that the Ueda reference specifically teaches "a multi layer flexible substrate (FPC2) with its electrical connection through anisotropic film (ACF1)". (See page 2 of the Action). It is respectfully submitted that the Ueda reference actually teaches "[a] multi-layered flexible substrate FPC2 is electrically connected with the multi-layered printed board PCB through the anisotropic conductive film ACF1." (emphasis added) (col. 19, lines 40-44). It is respectfully noted that "[a] substrate...electrically connected with [a] multi-layered printed board PCB through the anisotropic conductive film ACF1" does not read on "a laminar substrate with opposed sides, which opposed sides are both provided with electrically conducting patterns that are electrically through-connected via at least one opening in the laminar substrate, wherein said at least one opening is proximate said pixels."

It is further respectfully noted that the Ueda reference

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specifically teaches that the foregoing electric connection is performed "by adhering an anisotropic conductive film ACF to the connection portions JN1 and JN2 of the substrate PCB, by temporarily fixing the holes FHL of the substrates FPC2 and FPC3 on the positioning pins of a jig, and by coarsely aligning a hole CJH and a hole FJH of the FPC3." (emphasis added) (col. 19, lines 45-49).

The Action yet still further suggests (4) that the Burdis reference teaches "the use of one laminar substrate with an electrically conducting film, on which layers are carried on". (See page 2 of the Action). It is respectfully noted that the Burdis reference actually teaches "one laminar substrate covered on one side with an electrically conducting film, the layers being carried on this film covered side with a further electrically conducting film applied over the exposed layer." (col. 1, lines 16-19). It is also respectfully submitted that the Burdis reference, like the Ueda reference, fails to disclose or suggest "a laminar substrate with opposed sides, which opposed sides are both provided with electrically conducting patterns that are electrically through-connected via at least one opening in the laminar substrate, wherein said at least one opening is proximate said pixels."

Accordingly, based at least on the foregoing, reconsideration and withdrawal of the rejection, and allowance of claim 1, are respectfully requested.

With regard to present claims 2 through 10, which either directly or indirectly depend from claim 1, it is respectfully submitted that each of these claims are patentable at least for the reasons noted above with respect to claim 1. Accordingly,

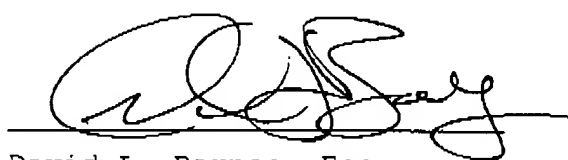
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reconsideration and withdrawal of the rejection, and allowance of claims 2 to 10, are respectfully requested.

In sum, it is respectfully submitted that the present claims are patentable over each of the cited references and/or any proper combination thereof. Hence, this application is in condition for allowance. Accordingly, reconsideration and withdrawal of all objections, and all rejections of the claims, are respectfully requested.

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